IOSR Journal of Engineering (IOSRJEN) **www.iosrjen.org**
ISSN (e): 2250-3021, ISSN (p): 2278-8719
PP 20-28

A Novel Transformer Less Interleaved Four Phase High Step Down Dc Converter

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Abstract: *For low output voltage, high output current systems applications, Synchronous switching power converters give better performance than non synchronous converters. This paper presents an interleaved synchronous buck converter which has low switch voltage stress with high conversion ratio. The input current can be shared among the inductors so that high reliability and efficiency can be obtained and ripples also reduced, the converter performance can be improved. Thus converter features automatic uniform current sharing characteristic of the interleaved phases without adding extra circuitry or complex control methods. Capacitors switching circuits are combined with interleaved four-phase buck converter for getting a high step-down conversion ratio without adopting an extreme short duty ratio. Synchronous rectifier technology is adopted to increase the converter efficiency. A 30V input voltage, 1.8V output voltage, circuit is simulated to verify the performance. The simulation is done in MATLAB/SIMULINK R 2012a.*

Keywords: *Buck Converter, Four phase, Interleaved, MATLAB/SIMULINK, transformer-less*

I. Introduction

The DC-to-DC converter is an electronic circuit or electromechanical device that converts a source of direct current (DC) from one voltage level to another. It is a type of electric power converter. Power levels range from very low (small batteries) to very high (high-voltage power transmission).In these DC-to-DC converters, energy is periodically stored within and released from a magnetic field in an inductor or a transformer, typically within a frequency range of 300kHz to 10MHz. By adjusting the duty cycle of the charging voltage (that is, the ratio of the on/off times), the amount of power transferred to a load can be more easily controlled, though this control can also be applied to the input current, the output current, or to maintain constant power. Transformer-based converters may provide isolation between input and output. In general, the term DC-to-DC converter refers to one of these switching converters. These circuits are the heart of a switched-mode power supply.

A basic buck converter is a voltage step down and current step up converter. It is mainly used in applications such as dc motor speed control and regulated dc supplies. It is also useful for tasks such as converting the main voltage in a computer down to the voltage needed by the processor. It has high efficiency due to no energy conversion. It has low switch current than load current. It has a disadvantage of ripples and during turn off current decays to zero.

In places where non isolation, step down conversion ratio and high output current with low ripple interleaved buck converter is used. It has a simple structure. Interleaving adds additional benefits such as reduced ripple currents in both the input and output circuits. In interleaved buck converter, all semi-converter devices suffer from the input voltage and hence high voltage devices rated above the input voltage should be used. High-voltage-rated devices have generally poor characteristics such as high cost, high on-resistance, high forward voltage drop, severe reverse recovery, etc. In addition, the converter operates under hard switching condition. Thus, the cost becomes high and the efficiency becomes poor. Higher efficiency is realized by splitting the output current into two paths, substantially reducing losses. To achieve high power density and better dynamics, it is required that the converter operates at higher switching frequency. But high switching frequency increases the switching losses. Therefore the efficiency is deteriorated.

The proposed Buck converter is like to the preceding conventional buck converter, excluding the diode is connected in parallel with a new transistor.By dropping the diodes voltage drop, the overall productivity for the buck converter can be enhanced. The synchronous rectifier needs another PWM signal that is the counterpart of the main PWM signal. S1 is on once diode D1 is off and reverse is true. This pwm arrangement is called Complementary PWM. Power losses in the proposed IBC are divided in three categories: load dependant conduction losses, frequency dependant switching losses and additional losses (including gate drive loss).

1.1 Background

1) Conventional interleaved buck converter: An interleaved buck converter (IBC) having low switching losses and improved step-down conversion ratio is proposed in [1] .The conventional IBC is shown in fig 1. This is

required to operating at high switching frequency.so the switching loss and conduction loss increses , which will decrease the overall efficiency of the circuit.

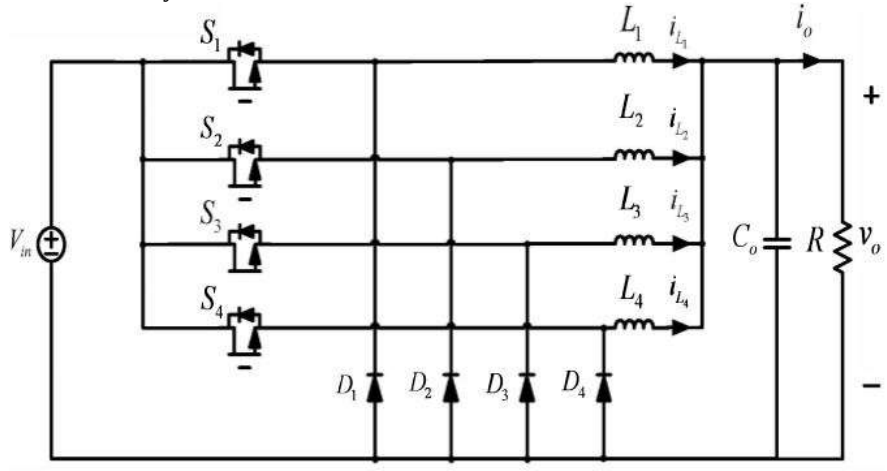

Fig.1 conventional interleaved buck converter

2) Extended Duty Ratio Interleaved Buck Converter: A review on "Multiphase Buck Converters with Extended Duty Cycle," is presented in [2].An extended duty ratio IBC is shown in fig 2. It have an efficient voltage divider. The only disadvantage of this circuit are

1. There is no uniform current sharing
2. Voltage stress is high

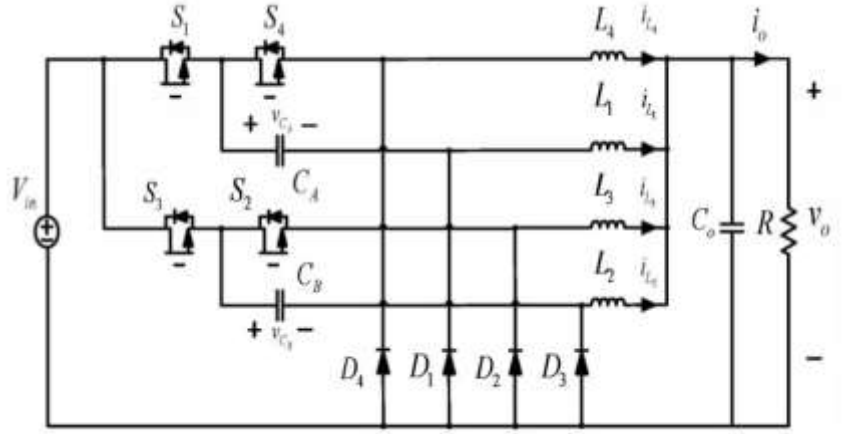

Fig.2 Extended duty ratio interleaved buck converter

II. Circuit ANALYSIS

The proposed novel transformer-less interleaved four-phase high step-down converter is shown in Fig.3, which is derived from two-phase extended duty ratio interleaved buck converter in. In order to further reduce input current ripple and output voltage ripple, the converter is divided into four-phase small inductors via interleaved operation to minimize those ripples. From Fig 3. one can see that the proposed converter consists of four inductors, four active power switches, four diodes and four capacitors. The main objectives of the new voltage divider circuit are twofold. First, they are used to store energy as usual. Second, based on the capacitive voltage division principle, they are used to reduce the voltage stress of active switches as well as increasing the step-down conversion ratio.

For the theoretical analysis, it will be considered that input and output voltages are ripple free, and all devices are ideal. The system is under steady state and operating in continuous conduction mode (CCM) with duty ratio being less than 0.5 for high step-down conversion ratio purpose.

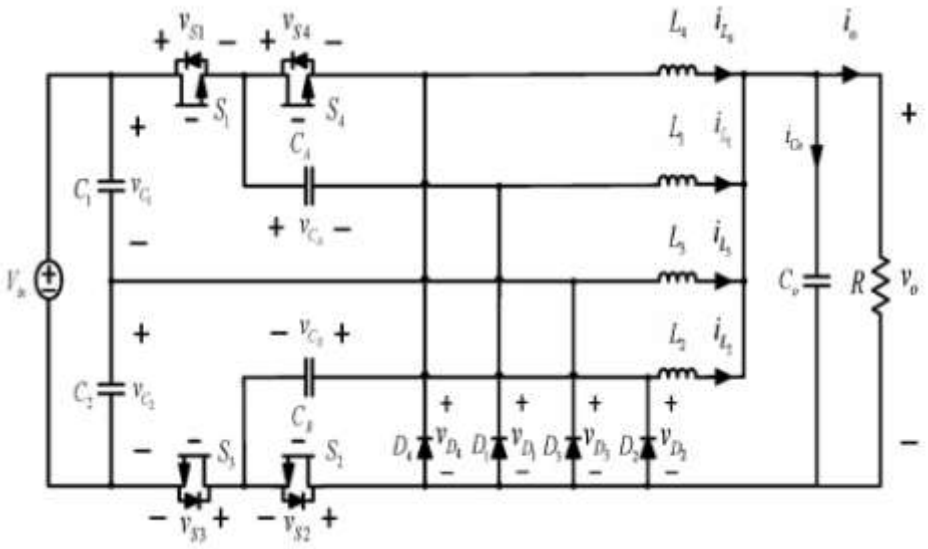

Fig.3 Proposed interleaved buck converter

1.1 Modes of Operation

This chapter describes the operating modes of the proposed converter. MODE 1 ($t_0 < t \leq t_1$): In this operation mode, switch S1 is turned on, switch S_2, S_3 and S_4 remain off. Hence, Diode D_1 becomes turned off and diode D_2, D_3 and D_4 remain on. The corresponding equivalent circuit is shown in Fig 4 . it is seen that the stored energy of C1 is discharged to C_A, L_1, and output load and current i_{L2}, i_{L3} and i_{L4} are freewheeling throughD_2, D_3 andD_4 respectively. TheV_{l2},V_{L3} and V_{L4} are equal to $-V_{CO}$, and hence, i_{L2}. i_{L3} and i_{L4} decrease linearly. The voltage across diode D_1 is clamped to V_{C1} minus V_{CA}. The voltage across switch S_3 is clamped toV_{C2} minusV_{CB} and the voltage across the switchS_2 and S_4 are clamped to V_{CB} and V_{C1} respectively.

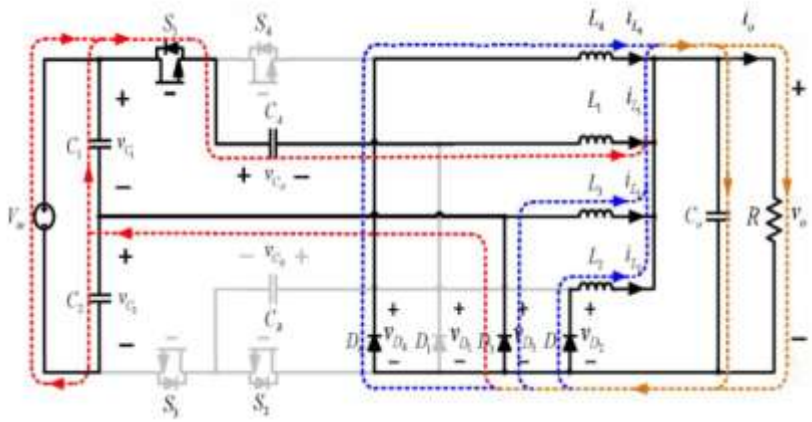

Fig.4 Proposed interleaved buck converter

MODE 2,4,6,8 ($t_{k-1} < t \leq t_k$): For this operation mode, the switch of S_1, S_2, S_3 and S_4 are off. The corresponding equivalent circuit is shown in Fig 5 . In this iLl, iL2, iL3 andiL4 are freewheeling through D_1, D_2, D_3 and D_4 respectively. All V_{Ll}, V_{Ll},VL3andV_{L4} are equal to$-V_{CO}$, and hence i_Ll, i_{L2},i_{L3} and i_{L4} decrease linearly. During this mode, the voltage across S_1, namelyV_1, is equal to the difference of V_{C1} andV_{CA}, and V_{S2} is clamped at V_{CB}. Similarly, the voltage across S_3, namely V_{S3}, is equal to the difference of V_{C2} and V_{CB}, and V_{S4} is clamped at V_{CA}

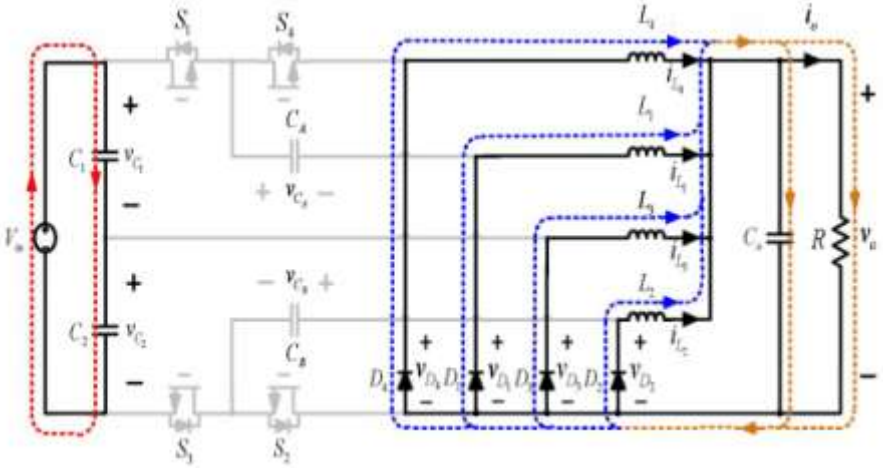

Fig.5 Proposed interleaved buck converter

MODE 3 (t_2<t ≤ t_3) : During this mode,D_2 becomes turned off while S_2 is turned on. The corresponding equivalent circuit is shown in Fig 3.4 . From this one can see that the stored energy of CB is discharged to L2 and output load and i_{Ll}, i_{L3} and i_{L4} are freewheeling throughD_1,D_3, and D_4 respectively. The inductor L_1,L_3, and L_4 are releasing energy to output load. The voltage across diode D_2 is clamped to V_{CB}. The voltage across switchS1 is clamped to V_{C1} minus V_{CA} and the voltage across the switchS_3 and S_4 are clamped to V_{C2} and V_{CA} respectively.

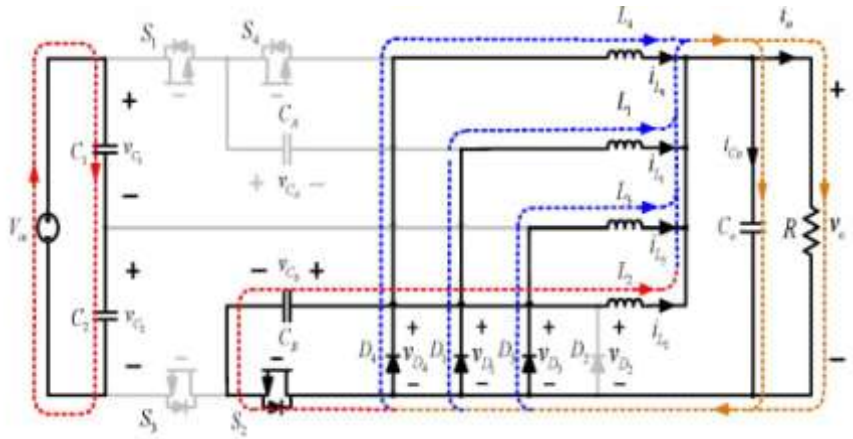

Fig.6 Proposed interleaved buck converter

MODE 5 (t_4 ≤ t ≤ t_5) : During this mode, D_4 becomes turned off while S_4 is turned on. The corresponding equivalent circuit is shown in Fig 7 . Here the stored energy of C_A is discharged toL_4 and output load and i_{Ll}, i_{L2} andi_{L3} are freewheeling through D_1,D_2, and D_3 respectively. The inductor L_1, L_2, and L_3 are releasing energy to output load. The voltage across diodesD_4 is clamped to V_{CA}. The voltage across switch S_1 is clamped toV_{C1} minusV_{CA} and the voltage across the switchS_2 and S_3 are clamped to V_{CB} andV_{C2} minus V_{CB} respectively.

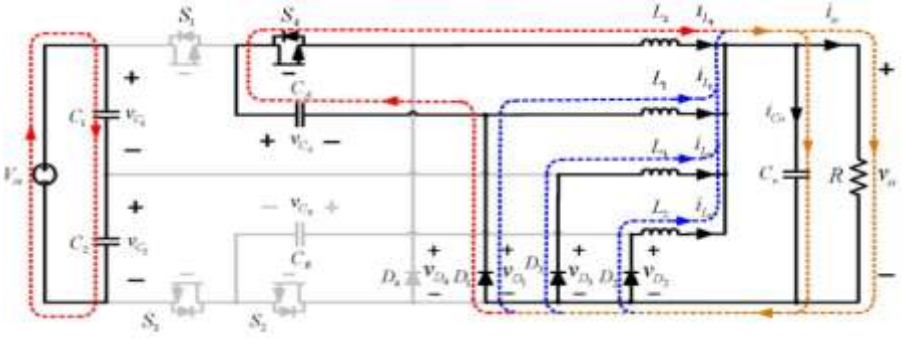

Fig.7 Proposed interleaved buck converter

MODE 7 ($t_6 < t \leq t_7$) : During this mode, D_3 becomes turned off whileS_3 is turned on. The corresponding equivalent circuit is shown in Fig 8 . Here the stored energy ofC_2 is discharged to C_B,L_3, and output load and i_{Ll}, i_{L2} and i_{L4} are freewheeling through D_1, D_2 and D_4 respectively. All V_{Ll},V_{L2} and V_{L4} are equal to $-V_{C0}$, and hence, i_{Ll}, i_{L2} and i_{L4} decrease linearly. The voltage across diode D_3 is clamped to V_{C2} minusV_{CB}. The voltage across switch S_1 is clamped toVin minus V_{CA} + V_{CB} and the voltage across the switch S_2 and S_4 are clamped to V_{CB} and V_{CA} respectively.

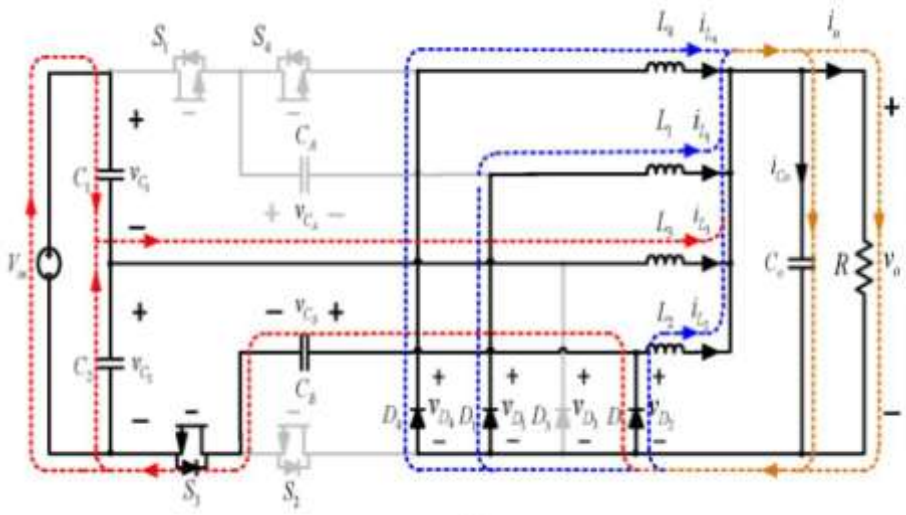

Fig.8 Proposed interleaved buck converter

III. Design

In order to simplify the circuit analysis of the proposed converter, some assumptions are made as follows.

1. All components are ideal components.
2. The capacitors are sufficiently large such that the voltages across them can consider as constant. Also, assume that C_l=C_2, C_A=C_B.
3. The system is under steady state and is operating in contineous conduction mode(CCM) and with duty ratio being less than 0.5 for high step ratio purpose.

A. Conversion Ratio

Referring to fig 4 - fig 8, from the volt-second relationship of the inductor L_1 - L_4 one can obtain the following relationships :

$(V_{C1} - V_{CA} - V_0) D - V_0 (1-D) = 0$ ……(1)
$(V_{CB} - V_0) D - V_0 (1-D) = 0$ ……(2)
$(V_{C2} - V_{CB} - V_0) D - V_0 (1-D) = 0$ …….(3)
$(V_{CA} - V_0) D - V_0 (1-D) = 0$ …….(4)

From equations 1 and 3 , voltage V_{C1} and V_{C2} can be derived as follow by substituting the V_{CA} and V_{CB} solutions of (2) and (4).

VC1 = (2 /D)V0 ……(5)
VC2 =(2 /D)V0 …… (6)

It follows from 5 and 6 that the output voltage can be obtained as below :

$V_{IN} = V_{C1} + V_{C2} = (4/D) V_0$ …….(7)

Thus the step down conversion ratio of the proposed converter can be obtained as follows :

$M_{stepdown} = (V_0/ Vin) = (D/4)$ ……(8)

B. Voltage Stresses On Semiconductor Components

From fig 4 - fig 8 ,we can see that the voltage stresses across the diodes D_1 - D_4 and switchesS_1,S_2,S_3andS_4 can be obtained directly as shown in the following equation .

$V_{D1max} = V_{D2max} = V_{D3max} = V_{D4max} = (V_{IN}/ 4)$ …(9)
$V_{S1max} = V_{S3max} = V_{S4max} = (Vin/ 2), V_{S2max} = (V_{IN} /4)$ …..(10)

From this we can conclude that, The proposed converter enables one to adopt lower voltage rating switches to further reduce both switching and conduction losses.

C. Characteristics Of Uniform Current Sharing

By using the state space averaging technique one can get the averaged state equations quite straightforward as follows:

$0 = D(-I_{l1} + I_{l3}) / (C1 + C2)$ ……(11)

$0 = D(I_{L1} - I_{L4})/ CA$ ……(12)

$0 = D(-I_{L2} + I_{L3}) / CB$ …….(13)

$0 = \{(I_{L1} + I_{L2} + I_{L3} + I_{L4})(R-VC0)\} / RC_0$ …..(14)

Where I0 = VC0 R The corresponding DC solution as follows

$I_{L1} = I_{L2} = I_{L3} = I_{L4} = I_0 /4$ …….(15)

From 15 we can conclude that the proposed converter possesses the inherent automatic uniform current sharing capability.

D. Output Current Ripples

The output current ripple can be derrived as follows:

$\Delta Iripple = D(1-4D) (Vin /4LFs) ,0 < D < 0.25$ (16)

The output current ripple of the proposed converter is affected by the input voltage,inductor value,switching duty ratio , and switching frequency. The normalized output current ripple of the proposed converter is given as follows :

$\Delta INripple = M(1-16M),0 < D < .25$ (17)

E. Performance Comparison

For demonstrating the performance of the proposed converter, the proposed converter is compared with conventional IBC and extended duty ratio IBC as shown in Table I.

Table I summarize the conversion ratio and normalized voltage stress of active as well as passive switches for reference. For comparison, the voltage stress is normalized by the input voltage Vin, the conversion ratio M, the normalized switch stresses and the normalized output diode stresses of the conventional IBC and the extended duty ratio IBC are also shown in the same table to provide better view. It is seen from Table I that the proposed converter can achieve higher step-down conversion ratio than that of the other two IBC converters. Therefore, the proposed converter is rather suitable for use in applications requiring high step down conversion ratio.

Table I: Comparison of steady state charecteristics

Gain/Stress	Conventional IBC	Extended duty ratio IBC	Proposed Converter
Conversion Ratio M	D	D/2	D/4
Voltage stress of the switches $S_{1,3}$	1	1/2	S_1 1/2; S_2 1/2
Voltage stress of the switches $S_{2,4}$	1	1	S_3 1/4; S_4 1/2
Voltage stress of diodes	1	1/2	1/4
Automatic uniform current sharing	No	No	Yes

from this table we can conclude that the proposed converter can achieve the lowest voltage stress for the active switches and diodes. As a result, one can expect that with proper design the proposed converter can adopt switch components with lower voltage ratings to acheive higher efficiency.

IV. Simulation

The simulation of the conventional IBC,extended duty ratio IBC and proposed IBC are done by using the prototype with 400V input and 500W ratings .the switching frequencies are chosen to be 40kHz.

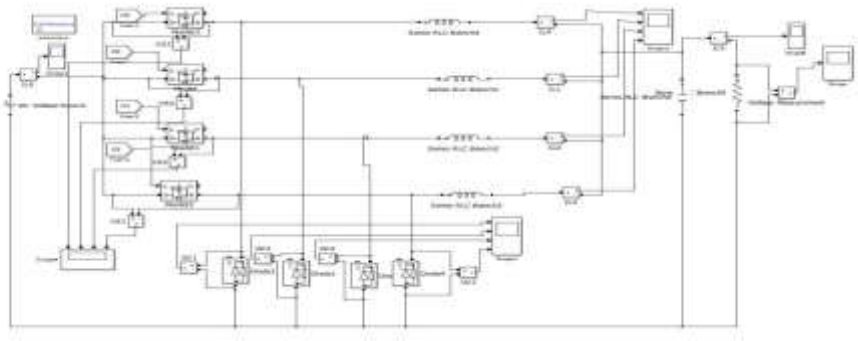

Fig.9 Simulink model of conventional IBC

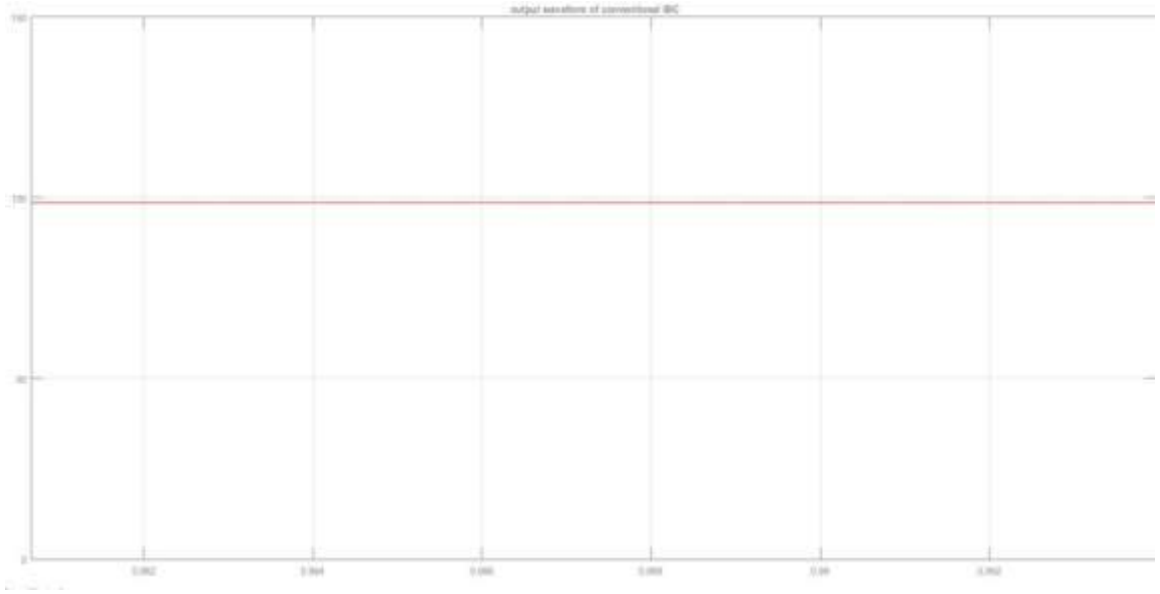

Fig.9 Output voltage of conventional IBC

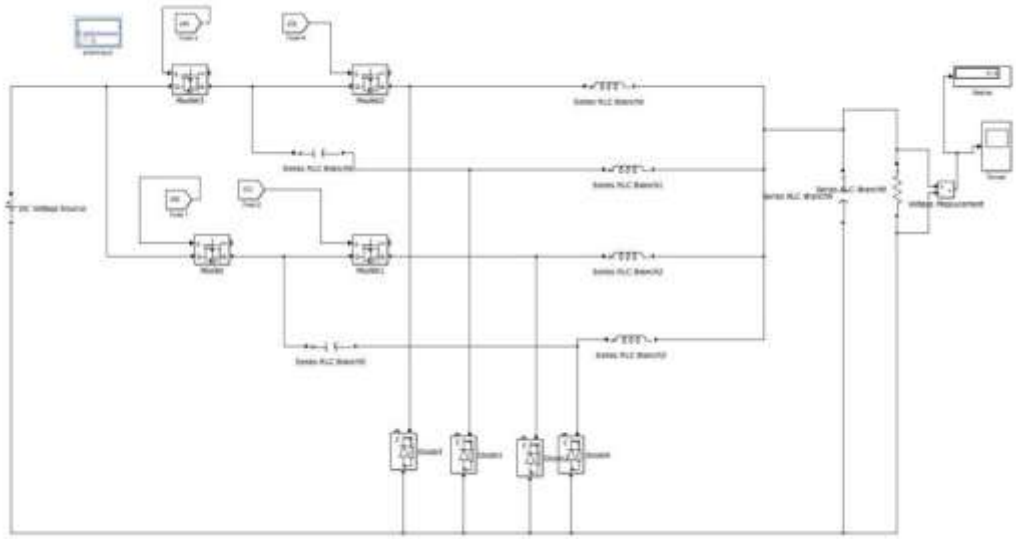

Fig.10 Simulink model of Extended duty ratio IBC

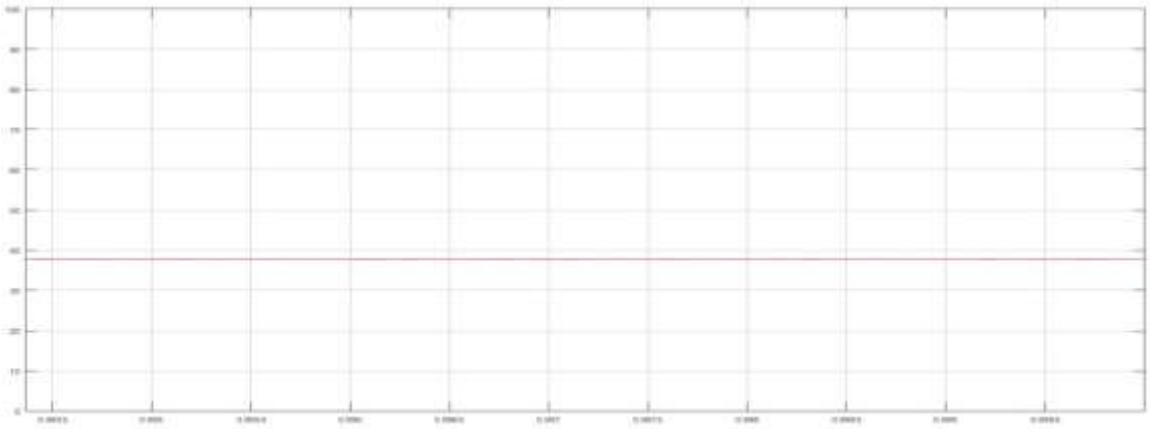

Fig.10 Output voltage of Extended duty ratio IBC

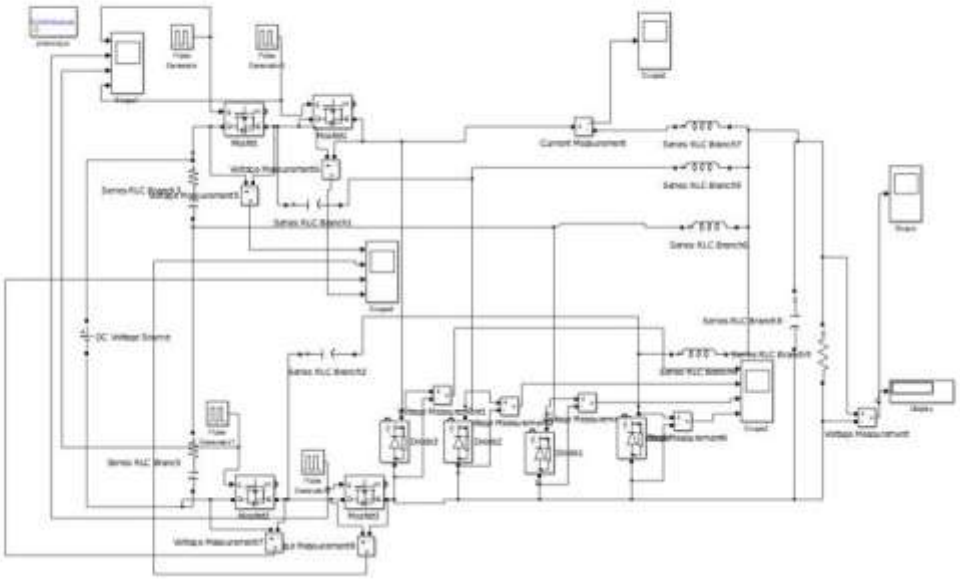

Fig.11 Simulink model of Proposed IBC

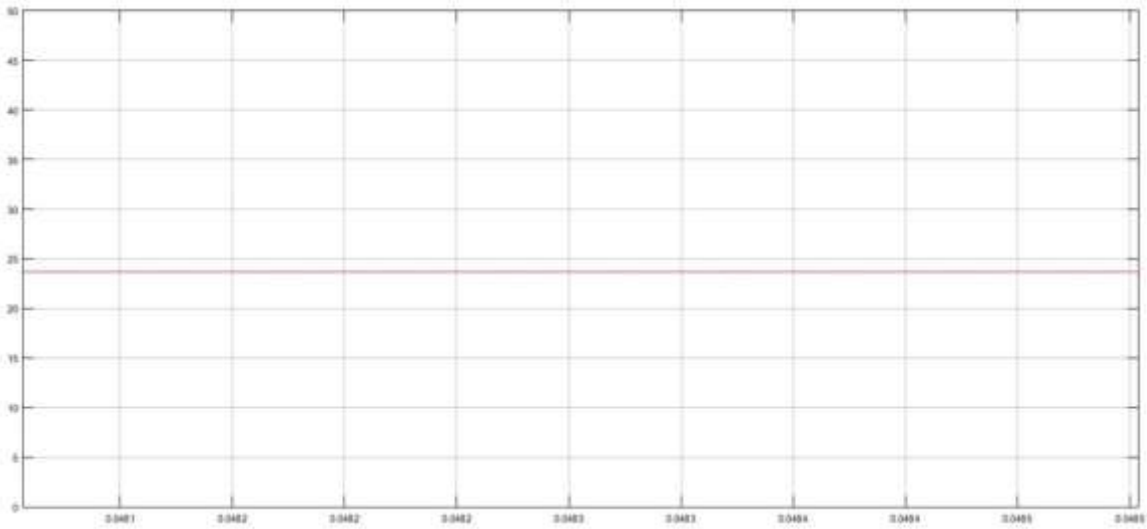

Fig.11 Output voltage of Proposed IBC

V. Conclusion

A novel transformer-less interleaved fourphase high step-down conversion ratio dc-dc converter with low switch voltage stress is proposed. In the proposed converter, the new capacitors switching circuits are combined with interleaved four-phase buck converter in order to get a high step-down conversion ratio. Based on the capacitive voltage division, the main objectives of the capacitors switching circuits in the converter are both storing energy in the blocking capacitors for increasing the voltage conversion ratio and reducing voltage stresses of active switches. As a result, the proposed converter topology possesses the low switch voltage stress characteristic. This will allow one to choose lower voltage rating MOSFETs to reduce both switching and conduction losses, and the overall efficiency is consequently improved. Tn addition, due to the charge balance of the blocking capacitor, the converter features automatic uniform current sharing characteristic of the interleaved phases without adding extra circuitry or complex control methods. The operating principle and steady-state analyses of the voltage gain are discussed.

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